1D Project Report

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# Introduction

This report shall be about the implementation of the 8-bit ALU in Multisim, and the different components required to build it. We will start with an elaboration of the different components and its operations, followed by our test results for the usability of the ALU, and improvements of design along with performance comparison of improved design.

# ALU

The ALU comprises of 4 large operational units connected to the output through a 4 way multiplexer. The unit takes in the following inputs:

|  |  |  |  |
| --- | --- | --- | --- |
| Variable | Input | Most Significant Bit (MSB) | Netlist names |
| A | GPIO 0 – GPIO 7 | GPIO 7 | A0 – A7 |
| B | GPIO 16 – GPIO 23 | GPIO 23 | B0 – B7 |
| ALUFN | SW 0 – SW 6 | SW 6 | ALUFN0 – ALUFN5 |

|  |  |
| --- | --- |
| Operation | ALUFN[5:0] |
| ADD | 000000 |
| SUB | 000001 |
| MUL | 000010 |
| AND | 011000 |
| OR | 011110 |
| XOR | 010110 |
| “A” (LDR) | 011010 |
| SHL | 100000 |
| SHR | 100001 |
| SRA | 100011 |
| CMPEQ | 110011 |
| CMPLT | 110101 |
| CMPLE | 110111 |

Variables A and B are inputs of the function while ALUFN represents the operation code which is controlled by 6 switches, SW 0 to SW 6. This code determines the operation which will be enacted by the ALU. The table on the right shows the code corresponding to each operation the ALU is capable of.

The output of the ALU is a 8-bit integer represented by 8 LED lights found on the FPGA board. The MSB of the output is LED7.

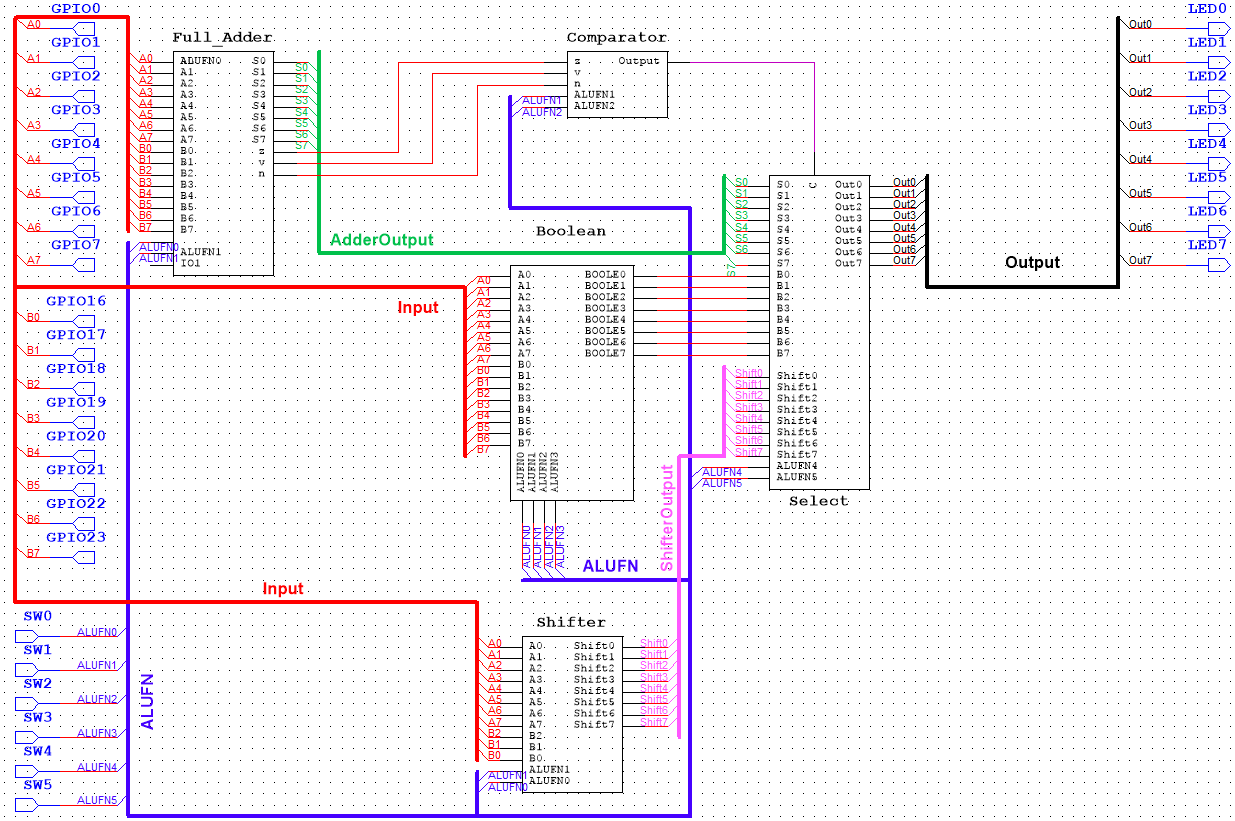


Diagram A1: ALU Schematics

## 8-bit Adder Unit

Function

* ADD, SUB, MUL
* Produces 3 signals: Z,V,N
  + Z is true when all outputs of the 8-bit results are zero
  + V is true when the addition operation overflows
  + N is true when the 8th bit is 1, meaning the result is a negative integer

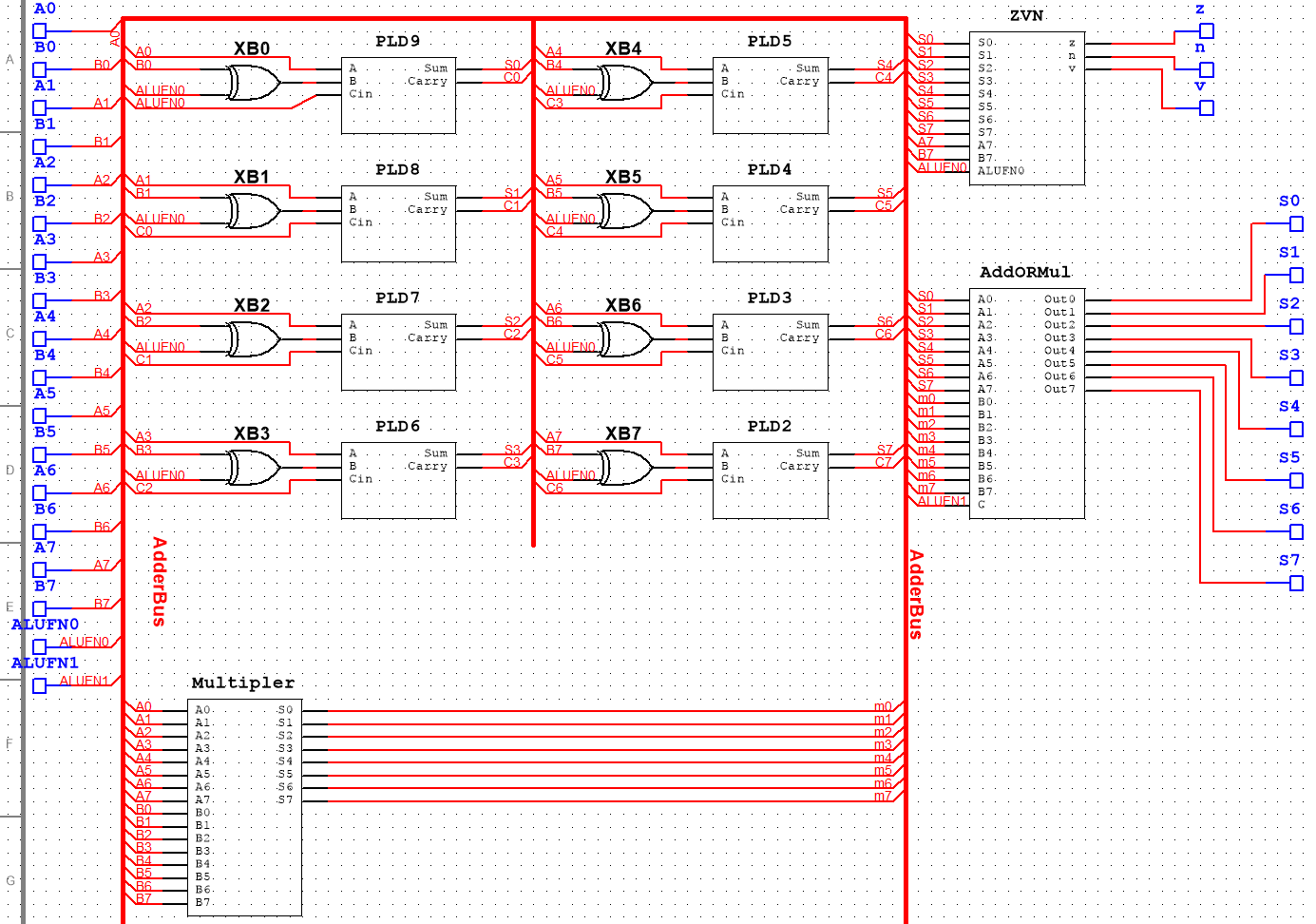


Diagram 1: Adder Schematics

As seen from the Multisim diagram, the 8-bit adder consists of 7 full adders being cascaded together through the carry. The last carry then becomes the 8th bit of the output. The output is then put through a 2 way multiplexer (AddORMul) which selects the correct output according to the operation code provided.

The Z output is computer using a series of ‘OR’ gates. The N output is the 8th bit of the cascaded full adders. V is computed using a combinational device that has the following characteristics:



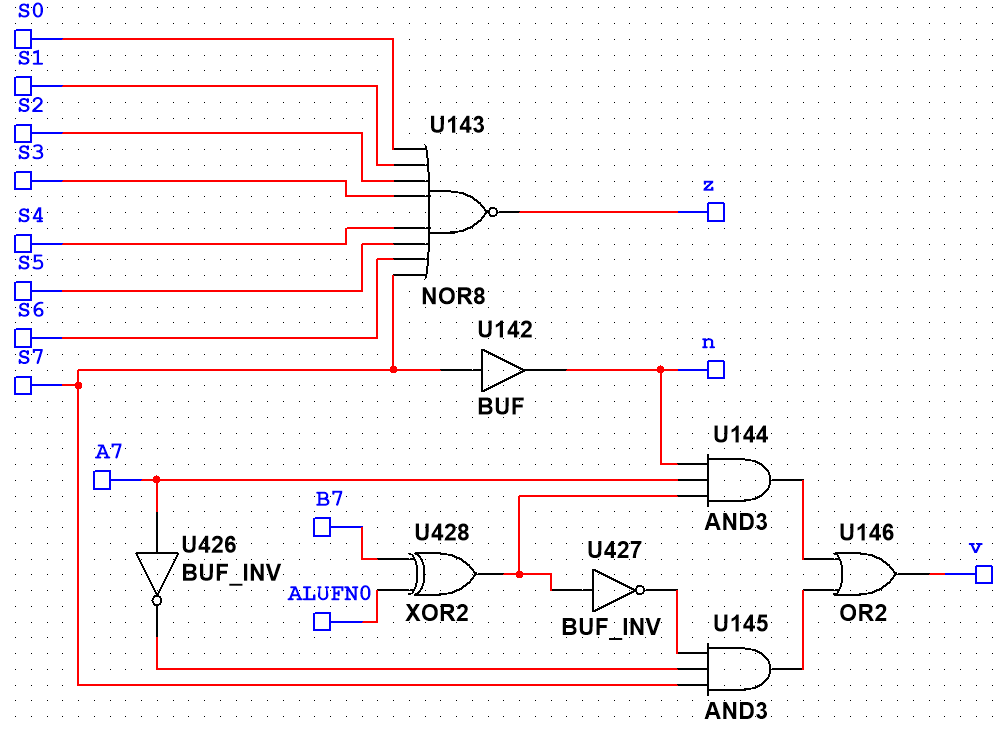


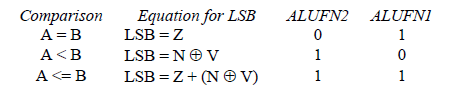
Diagram 2: ZVN Schematics

An AND logic unit serves as a single-bit multiplier. By using many AND gates to produce the partial products and summing them up with a cascade of adders, we can produce an 8-bit multiplier unit.

## 8-bit Compare Unit

Function:

* CMPEQ, CMPLT, CMPLE
* Checks for 3 statements depending on the ALUFN control signals input



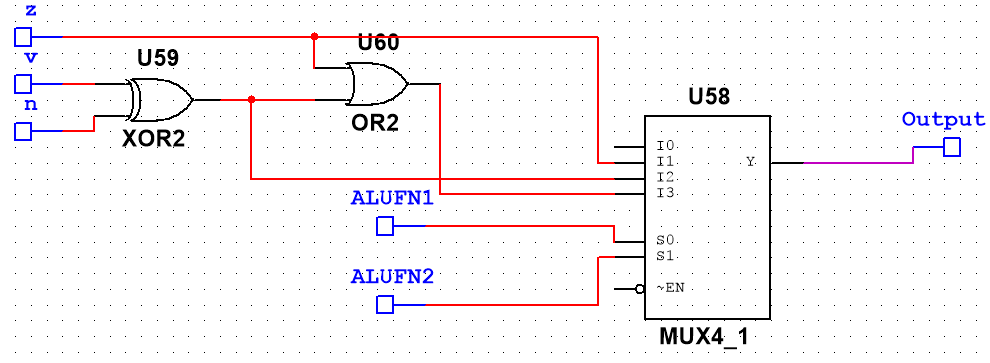


Diagram 3: Comparator Schematics

As seen from the diagram, the Compare unit consists of a mux4 that has control signals ALUFN1 and ALUFN2. The 4 inputs of the mux4 are output of the 3 boolean equation as shown above. The 4th input is a ground wire. Depending on the ALUFN signals, different inputs will be selected. The combination of ALUFN signals that selects a specific input are as show above as well. The output of the comparator unit is placed on the least significant bit while the rest of the bits are zeros.

## 8-bit Boolean Unit

Function:

* AND, OR, XOR, “A” (LDR)
* Takes 2 8-bit integers and compare them using the selected operation

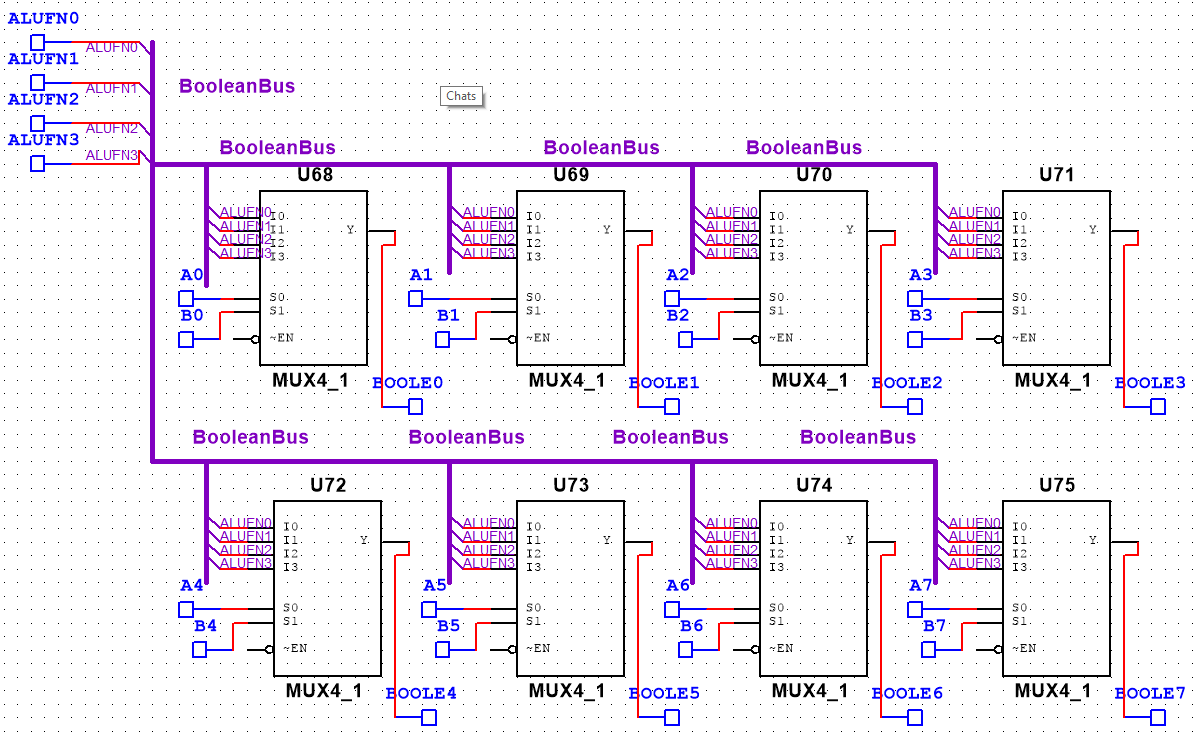


Diagram 4: Boolean Schematics

As seen from the diagram, the Boolean unit consists of 8 copies of a 4-to-1 multiplexer where ALUFN[0:3] encode the operation to be performed, and A and B are hooked to the selected inputs. The multiplexer can replicate any Boolean function by assigning the truth table values to the corresponding ALUFN input. The unit can perform up to 8 similar Boolean operations at once.

## 8-bit Shifter Unit

Function:

* SHL, SHR, SRA
* Operates 3 functions: shift left, shift right, and shift right arithmetic
  + Shift left shifts the bits by the amount specific and fills up the vacated bits with zeroes.
  + Shift right does the same as shift left but in the opposite direction
  + Shift right arithmetic fills the vacated bits with the 8th bit

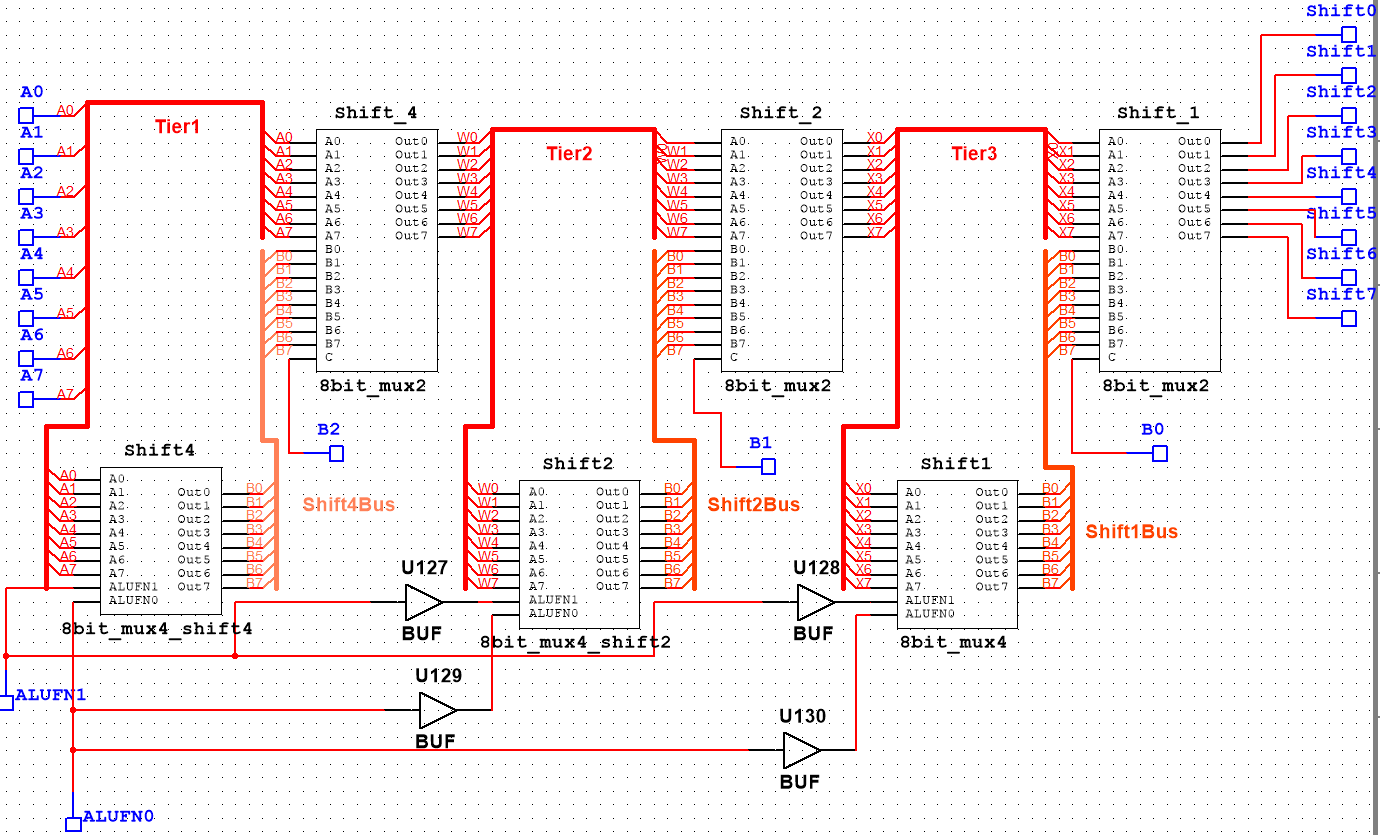


Diagram 5: Shifter Schematics

The shifter unit comprises of 3 tiers of multiplexers. Each tier is controlled by a single bit input from B and shifts a certain amount of bits in A. Within each tier is a 4 way multiplexer connected to a 2 way multiplexer. The 4 way multiplexer selects the correct shifting operation while the 2 way multiplexer determines if that tier will activated.